ABSTRACT

The invention provides processes for the formation of structures in microelectronic devices such as integrated circuit devices. More particularly, the invention relates to the formation of vias, interconnect metallization and wiring lines using multiple low dielectric-constant inter-metal dielectrics. The processes use two or more dissimilar low-k dielectrics for the inter-metal dielectrics of Cu-based dual damascene backends of integrated circuits. The use of both organic and inorganic low-k dielectrics offers advantages due to the significantly different plasma etch characteristics of the two kinds of dielectrics. One dielectric serves as the etchstop in etching the other dielectric so that no additional etchstop layer is required. Exceptional performance is achieved due to the lower parasitic capacitance resulting from the use of low-k dielectrics. An integrated circuit structure is formed having a substrate; an inorganic layer on the substrate which is composed of a pattern of metal lines on the substrate and an inorganic dielectric on the substrate between the metal lines; and an organic layer on the inorganic layer which is composed of an organic dielectric having metal filled vias therethrough which connect to the metal lines of the inorganic layer.